High-Isolation W-Band MEMS Switches

Jad Rizk, Guan-Leng Tan, Jeremy B. Muldavin, and Gabriel M. Rebeiz

***Abstract*—This paper presents the design, fabrication and measurement of single, T-match and π-match W-band high-isolation MEMS shunt switches on silicon substrates. The single and T-match design result in -20 dB isolation over the 80–110 GHz range with an insertion loss of 0.25 ± 0.1 dB. The π-match design results in a reflection coefficient lower than -20 dB up to 100 GHz, and an isolation of -30 to -40 dB from 75 to 110 GHz (limited by leakage through the substrate). The associated insertion loss is 0.4 ± 0.1 dB at 90 GHz. To our knowledge, this is the first demonstration of high-performance MEMS switches at W-band frequencies.**

***Index Terms*—High-isolation, low-loss, MEMS, microwave, micromachining, millimeter-wave, switches.**

I. Introduction

MEMS switches have been recently demonstrated up to 50 GHz using shunt and series implementations [1]–[3]. Both designs result in very low insertion loss, around 0.05–0.15 dB up to 40 GHz. The shunt switch results in very high isolation at 30–40 GHz (30–35 dB), but its performance is limited by the down-state LC resonant frequency [4], [5] to around 60 GHz. The series switch with an up-state capacitance of 2–3 fF results in acceptable isolation at 40 GHz (-26 to -22 dB), but is not suitable for high-isolation W-band applications.

This paper presents the design, fabrication and measurement of high-isolation W-band shunt switches. Both the T-match and the π-match are used to reduce the reflection coefficient of the shunt switch in the up-state position. The MEMS switch down-state capacitance is 270–300 fF so as to result in an LC resonant frequency in the W-band range, thereby ensuring a high-isolation response. The π-match also results in very high isolation over the entire W-band range since two MEMS switches are employed. The insertion loss of the MEMS circuits are around 1 dB better than state-of-the-art PIN diode switches at W-band frequencies [6], [7].

II. T-Match Shunt Switches: Design and Measurements

Fig. 1 shows a CPW shunt capacitive MEMS switch and its CLR series equivalent circuit. When the switch is in the up-state position, the up-state capacitance is small (10–15 fF) and the switch has a very low insertion loss (less than 0.2 dB). When the switch is in the down-state position, the down-state capacitance is 250–400 fF. With a series inductance of 6–10 pH, the resulting down-state LC resonant frequency is 80–130 GHz. At the resonant frequency, the switch isolation is independent of the down-state capacitance and is limited to -34 to -40 dB by the series resistance of the switch ($R_s = 0.25$–$0.5\ \Omega$) [4]. Beyond the resonant frequency, the isolation is determined by the inductance of the bridge, and a lower inductance will result in better isolation over a wider frequency range [4], [5].

The W-band switch is fabricated on a 400-μm thick high-resistivity silicon wafer (2000–3000 Ω cm). The CPW lines dimensions are G/W/G = 25/35/25 μm (50 Ω), and are fabricated using a 2-μm thick gold layer, except under the MEMS bridge where it is 5000-Å thick. Fig. 2 shows the measured loss of the CPW line over the W-band range for two different wafers. The attenuation varies from 4 dB/cm to 10 dB/cm at 90 GHz, and is due to charge trapped in the SiO_2 layer located in the CPW gap. A lower attenuation can be achieved by etching the silicon oxide from the gap of the CPW lines [8], [9]. The calibration on wafer 1 was excellent with an accuracy of ± 0.03 dB in the measured S_{21} of a 50 Ω line up to 110 GHz. The calibration of wafer 2 resulted in ± 0.1 dB accuracy up to 90 GHz.

The CPW line dimensions *under* the bridge are G/W/G = 30/50/30 μm in order to achieve a larger electrode and a lower pull-down voltage. The bridge is fabricated using a 1.5-μm thick layer of sputtered gold, and is suspended 2.2 μm above the silicon nitride dielectric. The sacrificial layer is photoresist and the bridges were released using a critical point dryer system. The interlayer dielectric is 1500 Å of silicon nitride ($\epsilon_r = 7.5$). In all designs, the MEMS bridge width is 40 μm. The pull-down voltage was 30 V.

Fig. 3 presents measurements done on a single CPW MEMS switch in the up and down-state positions. The reflection coefficient in the up-state is less than -16 dB over the entire W-Band range and fits an up-state capacitance of $C_u = 10$ fF. The corresponding parallel-plate capacitance C_{pp} is 8 fF for a gap height of 2.2 μm. The difference between the parallel-plate capacitance and the measured value is due to the fringing fields which result in a 30–40% increase in the MEMS bridge capacitance [4].

By adding small sections of high impedance lines on either side of the bridge, one can match the MEMS bridge in the up-state position over the whole W-band range [10]. This is equivalent to a T-match where the inductance L_m is given by $L_m = C_u Z_o^2/2$ and the equivalent high-impedance (Z_m) line length is $l = L_m v_p / Z_m$, where v_p is the velocity of the wave in the CPW lines. This is an approximate solution and the final values are obtained using LIBRA and are $\ell = 60$ μm for $Z_m = 60\ \Omega$.

Measurements in the up-state position for a T-match circuit are also shown in Fig. 3, and result in an excellent reflection loss ($S_{11} \leq -20$ dB) up to 110 GHz. The measured loss in the up-state position for the T-match circuit is 0.4 dB at

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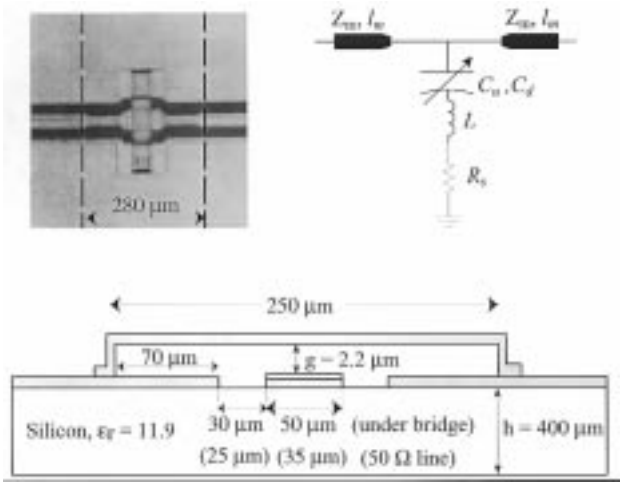

Fig. 1. CPW shunt capacitive MEMS switch and its equivalent circuit.

90 GHz. Knowing that the line loss is 10 dB/cm at 90 GHz and that the reference planes are 280 μm apart, the estimated loss in the up-state position is 0.28 dB at 90 GHz. For wafer 2 with 4.3 dB/cm loss at 90 GHz, the measured loss was 0.25 ± 0.1 dB (not shown). The single MEMS bridge (with no T-match) results in 0.20 dB loss at 90 GHz when fabricated on wafer 2. The corresponding calibration planes were 135 μm apart.

For the down-state position, Fig. 3 shows measurements for a single bridge with T-matching. The no-match case results in a nearly identical response and is not shown. The fitted values are $C_d = 270 \pm 10$ fF, $L = 8$–9 pH, and $R_s = 0.5\ \Omega$. It is hard to fit L and R_s well due to measured isolation accuracy. The design results in a -20 dB isolation from 80 GHz to more than 110 GHz. The equivalent down-state parallel plate capacitance is equal to $C_{ppd} = \epsilon_r \epsilon_o (A/d) = 890$ fF and the measured down-state capacitance is $C_d = 0.3 C_{ppd}$. This is due to the surface roughness of the MEMS bridge and the silicon nitride layer. The measured C_d/C_u ratio is 27. The reduction in the down-state capacitance is actually beneficial to W-band switches since it results in an LC resonant frequency of 100–105 GHz. If the capacitance is 900 fF, the resonant frequency would be 60 GHz and the W-band performance will be degraded.

III. π-Match Shunt Switches; Design and Measurements

The isolation of the W-band CPW MEMS shunt switch can be significantly improved if a π-circuit is used (Fig. 4). The circuit consists of two MEMS switches connected by a *short* high-impedance t-line. The π-circuit does two functions: First, it provides an excellent match in the up-state position over a wide bandwidth. Second, the combination of the two shunt switches in parallel results in a wide isolation bandwidth. The value of the matching inductance can be derived to be: $L_m = 2C_u Z_o^2$. For $C_u = 10$–15 fF, $L_m = 50$–75 pH and the equivalent 60 Ω-line length is 100–150 μm.

Fig. 5 presents measurements for a π-circuit for $l = 180$ μm. Due to a mistake, $l = 130$ μm was not placed on the mask. The up-state reflection coefficient is less than -15 dB up to 110 GHz and can be improved by tuning the length of the high-impedance line (should be made shorter). The equivalent up-state capacitance for the single MEMS bridge is 10 ± 1 fF, and is consistent

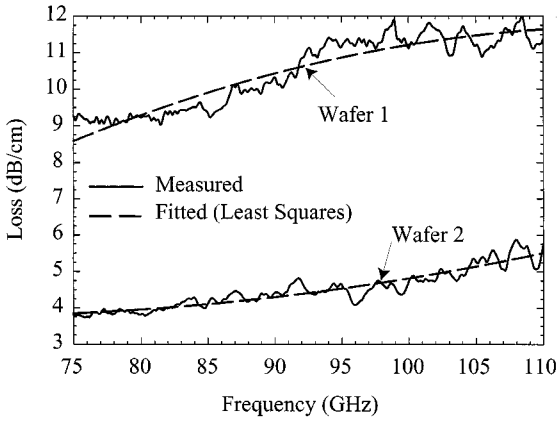

Fig. 2. Loss in dB/cm for a 50 Ω CPW line (G/W/G = 25/35/25 μm) on a 400-μm silicon substrate as function of frequency.

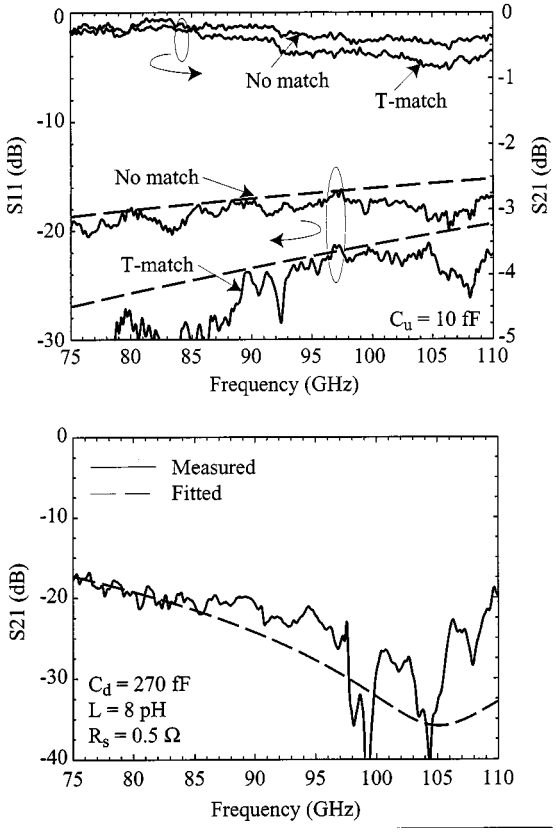

Fig. 3. Measured S-parameters of a T-match switch: (top) in the up-state position and, (bottom) in the down-state position.

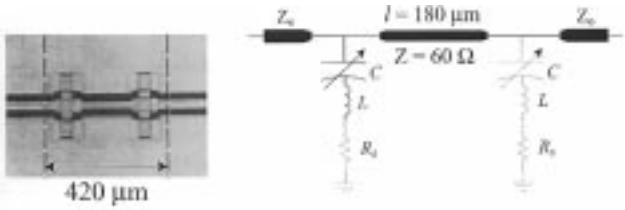

Fig. 4. π-circuit with CPW shunt capacitive MEMS switches, and its equivalent circuit.

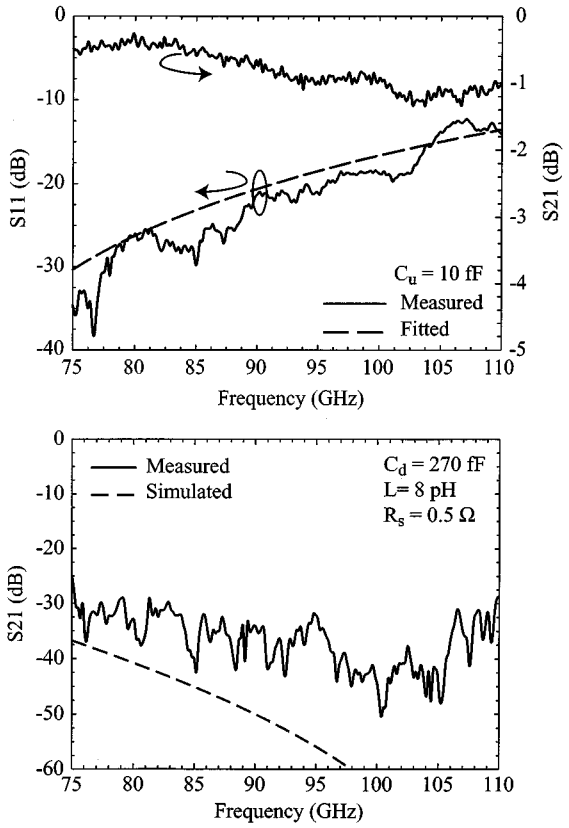

Fig. 5. Measured S-parameters of a π-circuit: (top) in the up-state position and, (bottom) in the down-state position.

with the capacitance values found for the one-bridge design. The measured loss is 0.7 dB at 90 GHz. With a line loss of 10 dB/cm at 90 GHz (wafer 1) and reference planes 420 μm apart, the estimated loss for the π-circuit is 0.42 dB at 90 GHz. The difference is due to the higher loss in the 60 Ω t-line section. The measured loss for wafer 2 with 4.3 dB/cm at 90 GHz is 0.4 ± 0.1 dB (not shown).

Fig. 5 shows the measured S-parameters for MEMS bridges pulled down with a bias voltage of 30 V. The π-match circuit results in an isolation better than -30 dB over the entire W-band frequency range. In fact, the measured isolation for a π-design with *pulled-down* bridges and a π-design with *fabricated-down* bridges were identical. Therefore, the isolation measurement is limited by the leakage in the substrate. The simulated response with $C_d = 270$ fF, $L = 8$ pH, and $R_s = 0.5\ \Omega$ shows a much higher isolation but could not be measured. The π-circuit results in excellent response for a large range of down-state capacitance or bridge inductance values, and is recommended for high-isolation W-band designs.

IV. Conclusion

This paper presented single, T-match, and π-match MEMS switches for W-band applications. It is seen that all the designs result in a very low reflection coefficient up to 110 GHz for an up-state capacitance of $C_u = 10$ fF. However, the π-match design results in 15–30 dB better isolation than the single or T-match switch. In fact, the isolation of a π-match design is so low that it is limited by the leakage through the substrate.

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